Docket No. 200308565-1

Amendments to the Claims:

Status of Claims:

Claims 1 - 44 are pending for examination.

Claims N/A are added herein.

Claims N/A are canceled herein.

Claims 1, 17, 29, 35, 37, 38, 44 are in independent form.

Claims 1, 4-9, 13-29, 34, 35, 37-39, 41-44 are amended herein.

1. (Currently Amended) A system comprising:

a memory mapping logic configured to provide access to memory locations, where the memory mapping logic can be configured to direct a memory accessing operation intended for one memory location to another memory location; and

a memory quality assurance logic operably connected to the memory mapping logic, where the memory quality assurance logic is configured to:

control copying contents between a first plurality of memory locations and a second plurality of memory locations;

reconfigure the memory mapping logic so that memory accessing operations intended for the first plurality of memory locations are directed to the second plurality of memory locations; and

initiate memory testing of the first plurality of memory locations,

where the first plurality of memory locations is less than a page of memory and where the second plurality of memory locations is less than a page of memory,

where the memory mapping logic and the memory quality assurance logic do not consume operating system resources.

2. (Original) The system of claim 1, where the memory mapping logic includes a crossbar.

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3. (Original) The system of claim 1, where the memory mapping logic includes one or more address translation tables.

4. (Currently Amended) The system of claim 1, where the memory quality assurance logic is configured to select the first plurality of memory locations by one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method.

5. (Currently Amended) The system of claim 1, where the memory quality assurance logic is configured to selectively logically remove ~~the~~ a ~~first~~ memory location from the ~~a~~ first ~~set~~ plurality of memory locations by reconfiguring the memory mapping logic, based, at least in part, on a result from the memory testing of the ~~first~~ memory location.

6. (Currently Amended) The system of claim 1, where the memory quality assurance logic is configured to selectively logically replace ~~the~~ a first memory location with ~~the~~ a second memory location by reconfiguring the memory mapping logic, based, at least in part, on a result from the memory testing of the first memory location.

7. (Currently Amended) The system of claim 1, where the memory quality assurance logic is configured to selectively logically replace ~~the~~ a ~~first~~ memory location with another memory location from ~~a~~ first ~~set~~ plurality of memory locations by reconfiguring the memory mapping logic based, at least in part, on a result from the memory testing of the ~~first~~ memory location.

8. (Currently Amended) The system of claim 1, where the memory quality assurance logic is configured to initiate memory testing of the first plurality of memory locations by sending one or more signals to a memory testing logic.

9. (Currently Amended) The system of claim 1, where the memory quality assurance logic is configured to initiate memory testing of the first plurality of memory locations by sending one

or more signals to an onboard memory testing logic, where the onboard memory testing logic is physically connected to the first plurality of memory locations.

10. (Original) The system of claim 1, where the memory quality assurance logic selects the second memory location.

11. (Original) The system of claim 1, where the memory quality assurance logic includes one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data.

12. (Original) The system of claim 1, where the memory quality assurance logic is operably connected to one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data.

13. (Currently Amended) The system of claim 1, where the second plurality of memory locations is located in internal memory of the memory mapping logic.

14. (Currently Amended) The system of claim 1, where the second plurality of memory locations is located in internal memory of the memory quality assurance logic.

15. (Currently Amended) The system of claim 1, where the second plurality of memory locations is physically connected to the first plurality of memory locations.

16. (Currently Amended) The system of claim 1, where the memory quality assurance logic is configured to select the second plurality of memory locations.

17. (Currently Amended) A method comprising:

selectively copying contents of a first plurality of memory locations to a second plurality of memory locations;

logically replacing the first plurality of memory locations with the second plurality of memory locations; and

initiating memory testing of the first plurality of memory locations without an operating system interaction and without consumption of operating system resources,

where the first plurality of memory locations is less than a page of memory and where the second plurality of memory locations is less than a page of memory.

18. (Currently Amended) The method of claim 17, where access to the contents of the first plurality of memory locations as copied to the second plurality of memory locations can continue concurrently with the memory testing.

19. (Currently Amended) The method of claim 17, where the memory testing of the first plurality of memory locations can continue without consuming a non-memory operating system resource.

20. (Currently Amended) The method of claim 17, comprising identifying the first plurality of memory locations by one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method.

21. (Currently Amended) The method of claim 17, where the first plurality of memory locations is logically replaced by the second plurality of memory locations by reconfiguring address resolving means.

22. (Currently Amended) The method of claim 17, comprising selectively logically removing the first plurality of memory locations ~~from a first set of memory~~.

23. (Currently Amended) The method of claim 17, comprising selectively logically replacing the first plurality of memory locations with a third plurality of memory locations, where the first plurality of memory locations and the third plurality of memory locations are physically located in the same memory apparatus.

24. (Currently Amended) The method of claim 17, comprising providing a report concerning a quality of the first plurality of memory locations, where the report is based, at least in part, on the testing of the first plurality of memory locations.

25. (Currently Amended) The method of claim 17, comprising storing a quality data associated with the quality of the first plurality of memory locations, where the quality data is based, at least in part, on the testing of the first plurality of memory locations.

26. (Currently Amended) The method of claim 17, where testing the first plurality of memory locations includes two or more test methods.

27. (Currently Amended) The method of claim 17, where the first plurality of memory locations can be tested by one or more of, a parity test, an electrical test, a striping test, a marching one test, a marching zero test, and a pattern test.

28. (Currently Amended) The method of claim 17, comprising selecting the second plurality of memory locations to logically replace the first plurality of memory locations.

29. (Currently Amended) A system, comprising:

a processor;

a memory operably connected to the processor, where the processor can access the memory;

a memory mapping logic configured to provide access to memory locations in the memory, where the memory mapping logic can be configured to direct a memory accessing operation intended for one memory location to another memory location; and

a memory quality assurance logic operably connected to the memory mapping logic, where the memory quality assurance logic is configured to:

control copying of contents between a first plurality of memory locations and a second plurality of memory locations;

reconfigure the memory mapping logic so that memory accessing operations intended for the first plurality of memory locations are directed to the second plurality of memory locations; and

initiate memory testing of the first plurality of memory locations,

where the first plurality of memory locations is less than a page of memory and where the second plurality of memory locations is less than a page of memory,

where the memory mapping logic and the memory quality assurance logic are transparent to an operating system.

30. (Original) The system of claim 29, where the system is embedded in a computer.

31. (Original) The system of claim 29, where the system is embedded in an image forming device.

32. (Original) The system of claim 29, where the memory quality assurance logic includes one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data.

33. (Original) The system of claim 29, where the memory quality assurance logic is operably connected to one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data.

34. (Currently Amended) The system of claim 29, comprising a memory location selection logic configured to select the first plurality of memory locations and the second plurality of memory locations.

35. (Currently Amended) A computer-readable medium storing processor executable instructions operable to perform a method, the method comprising:

selecting a first memory location to test from a first set of memory;

selectively copying contents of the first memory location to a second memory location of a second set of memory;

logically replacing the first memory location with the second memory location; and

initiating testing of the first memory location without consuming operating system resources,

where the first set of memory ~~location~~ is less than a page of memory and where the second set of memory ~~location~~ is less than a page of memory.

36. (Original) The computer-readable medium of claim 35, where the method comprises logically replacing the first memory location with the second memory location by reconfiguring address resolving means.

37. (Currently Amended) A system comprising:

means for logically replacing a testable memory location with a replacement memory location, where the means for logically replacing operates without interacting with an operating system;

means for testing the testable memory location, where the means for testing operates without interacting with an operating system; and

means for selectively logically removing the testable memory location from a set of memory based, at least in part, on a result of testing the testable memory location, where the means for selectively logically removing the testable memory location operates without interacting with an operating system,

where the set of ~~testable~~ memory ~~location~~ is less than a page of memory,

where the means for logically replacing a testable memory location, the means for testing the testable memory location and the means for selectively logically removing the testable memory location do not consume operating system resources.

38. (Currently Amended) An operating system transparent system for on-the-fly memory testing, comprising:

a memory location identifying logic configured to identify a plurality of target memory locations and a plurality of replacement memory locations;

a programmable memory address resolving logic configured to provide access to the plurality of target memory locations and the plurality of replacement locations; and

a test controlling logic operably connected to the programmable memory address resolving logic, the test controlling logic configured to selectively program the programmable memory address resolving logic to divert memory accesses from the plurality of target memory locations to the plurality of replacement memory locations and to initiate testing of the plurality of target memory locations,

where the memory location identifying logic, the programmable memory address resolving logic, and the test controlling logic do not consume operating system resources,

where the plurality of target memory locations is less than a page of memory and where the plurality of replacement memory locations is less than a page of memory.

39. (Currently Amended) The system of claim 38, where the memory location identifying logic is configured to identify a the plurality of target memory locations using one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method.

40. (Previously Presented) The system of claim 38, where the programmable memory address resolving logic includes a crossbar.

41. (Currently Amended) The system of claim 38, where the test controlling logic is also configured to selectively reprogram the programmable memory address resolving logic to stop diverting memory accesses from the plurality of target memory locations to the plurality of replacement memory locations.

42. (Currently Amended) The system of claim 38, where the test controlling logic is also configured to logically remove the plurality of target memory locations from a pool of memory available to operating system instances without requiring an operating system instance to halt execution.

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43. (Currently Amended) The system of claim 42, where the test controlling logic logically removes the plurality of target memory locations from the pool of memory by reprogramming the programmable memory address resolving logic.

44. (Currently Amended) An operating system transparent method for on-the-fly memory testing, comprising:

identifying a plurality of test memory locations and a plurality of mirroring memory locations;

mirroring the test memory locations to the mirroring memory locations;

selectively reconfiguring memory accessing operations so that memory accesses originating in an operating system instance that are addressed to the plurality of test memory locations are redirected to the plurality of mirroring memory locations; and

testing the plurality of test memory locations without disrupting an operating system instance,

where the plurality of test memory locations is less than a page of memory and where the plurality of mirroring memory locations is less than a page of memory,

where the method is performed without consumption of operating system resources.